Final Report

The Virtual Time Machine

Award No. CCR-9096179, 1989-1993

Project Summary

This work studies a parallel machine architecture called the Virtual Time Machine (VTM) that uses rollback to synchronize parallel computations. A simulator for the machine architecture was developed, and performance of benchmark applications was examined. A software-based implementation on general purpose multiprocessor hardware (a Kendall Square Research KSR-1 machine) was developed, and used extensively to evaluate performance of this approach. Hardware designs for key components of the machine were developed, and an implementation of certain mechanisms used in the memory system was developed (in collaboration with *Integrated Parallel Technologies*) and formally verified. Extensive analytic and experimental performance studies using a testbed system running on a BBN Butterfly the KSR-1 architecture were completed. A parallelizing compiler for SIMSCRIPT II.5 was developed and demonstrated on both the simulated machine and the KSR-1 implementation.

The project successfully demonstrated the effectiveness of rollback-based synchronization for a variety of discrete event simulation applications. Rollback-based synchronization mechanisms appear to have good promise for providing orders of magnitude speedup for large-scale simulation computations that are too time consuming to perform today in applications such as computer system design, telecommunication networks, design of transportation systems, manufacturing, and others.

Software

A significant amount of parallel simulation software was developed for this project. This software is made available to anyone requesting it, free of charge. To our knowledge, at least two groups (at the University of Calgary and University of Waikato in New Zealand) are actively using this software in their research.

Publications

The following publications report results supported in whole or in part by research performed under this grant:

[1] J. J. Tsai and R. M. Fujimoto. Automatic parallelization of discrete event simulation programs. In *1993 Winter Simulation Conference Proceedings*, December 1993.

[2] G. Gopalakrishnan and R. M. Fujimoto. Design and verification of the rollback chip using hop: A case study of formal methods applied to hardware design. *ACM Transactions on Computer Systems*, 11(2), May 1993.

[3] V. K. Madisetti, D. A. Hardaker, and R. M. Fujimoto. The mimdix operating system for parallel simulation and supercomputing. *Journal of Parallel and Distributed Computing*, 18(4):473–483, August 1993.

[4] R. M. Fujimoto, J. Tsai, and G. Gopalakrishnan. Design and evaluation of the rollback chip: Special purpose hardware for Time Warp. *IEEE Transactions on Computers*, 41(1):68–82, January 1992.

[5] A. Gupta, I. F. Akyildiz, and R. M. Fujimoto. Performance analysis of Time Warp with multiple homogenous processors. *IEEE Transactions on Software Engineering*, 17(10):1013–1027, October 1991.

[6] K. Ghosh and R. M. Fujimoto. Parallel discrete event simulation using space-time memory. In *Proceedings of the 1991 International Conference on Parallel Processing*, volume 3, pages 201–208, August 1991.

[7] J. T. Gray, D. W. Reed, and M. R. Frank. Virtual time conversion hardware. Technical report, College of Computing, Georgia Tech, 1990.

[8] C. A. Buzzell, M. J. Robb, and R. M. Fujimoto. Modular VME rollback hardware for Time Warp. In *Proceedings of the SCS Multiconference on Distributed Simulation*, volume 22, pages 153–156. SCS Simulation Series, January 1990.

[9] R. M. Fujimoto. Performance of Time Warp under synthetic workloads. In *Proceedings of the SCS Multiconference on Distributed Simulation*, volume 22, pages 23–28. SCS Simulation Series, January 1990.